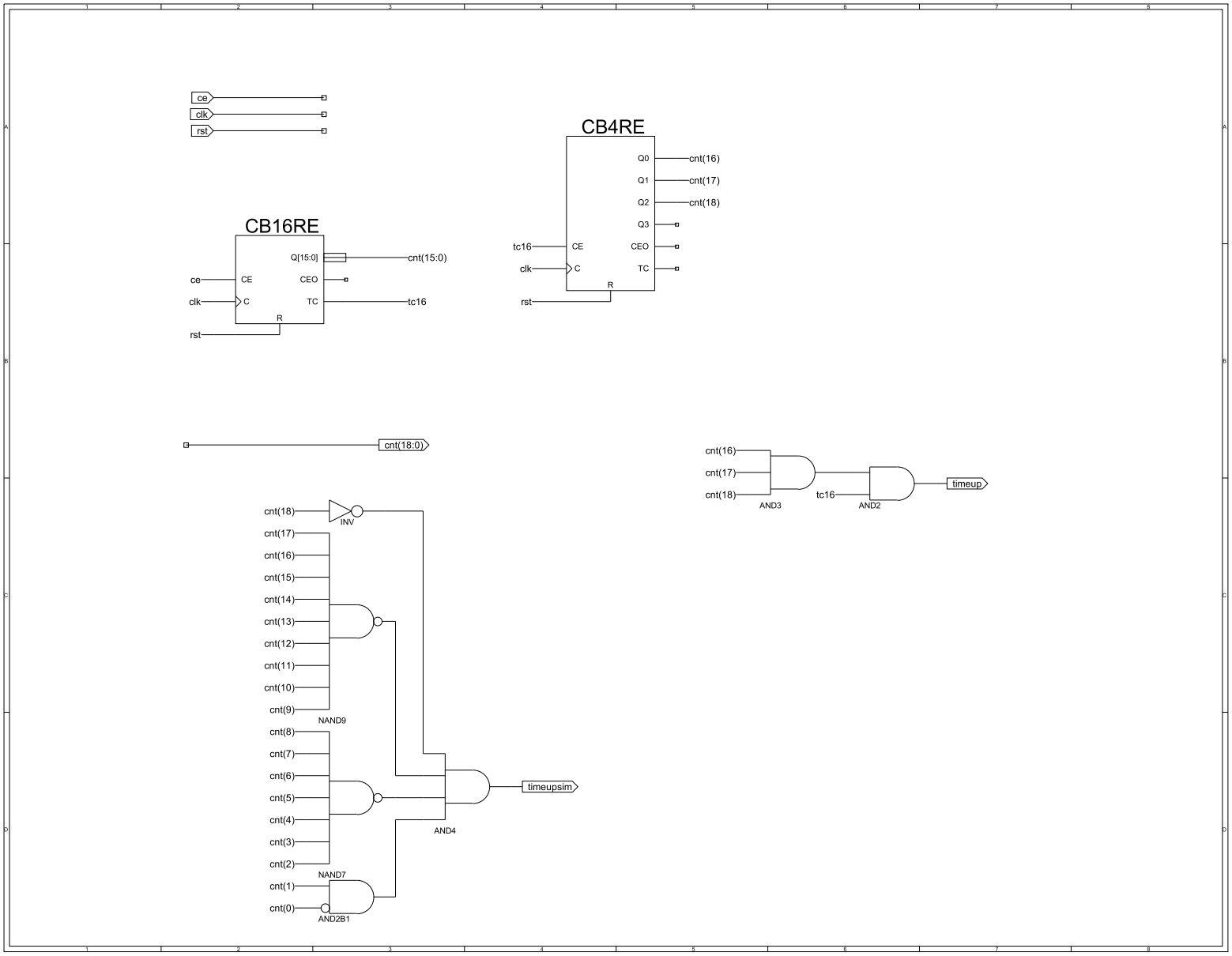
ce
clk
rst
CB16RE
Q[15:0]
cnt(15:0)
ce
CE
CEO
clk
C
TC
tc16
R
rst
CB4RE
Q0
cnt(16)
Q1
cnt(17)
Q2
cnt(18)
Q3
tc16
CE
CEO
clk
C
TC
R
rst
cnt(18:0)
cnt(16)
cnt(17)
cnt(18)
AND3
tc16
AND2
timeup
cnt(18)
INV
cnt(17)
cnt(16)
cnt(15)
cnt(14)
cnt(13)
cnt(12)
cnt(11)
cnt(10)
cnt(9)
NAND9
cnt(8)
cnt(7)
cnt(6)
cnt(5)
cnt(4)
cnt(3)
cnt(2)
NAND7
cnt(1)
cnt(0)
AND2B1
AND4
timeupsim