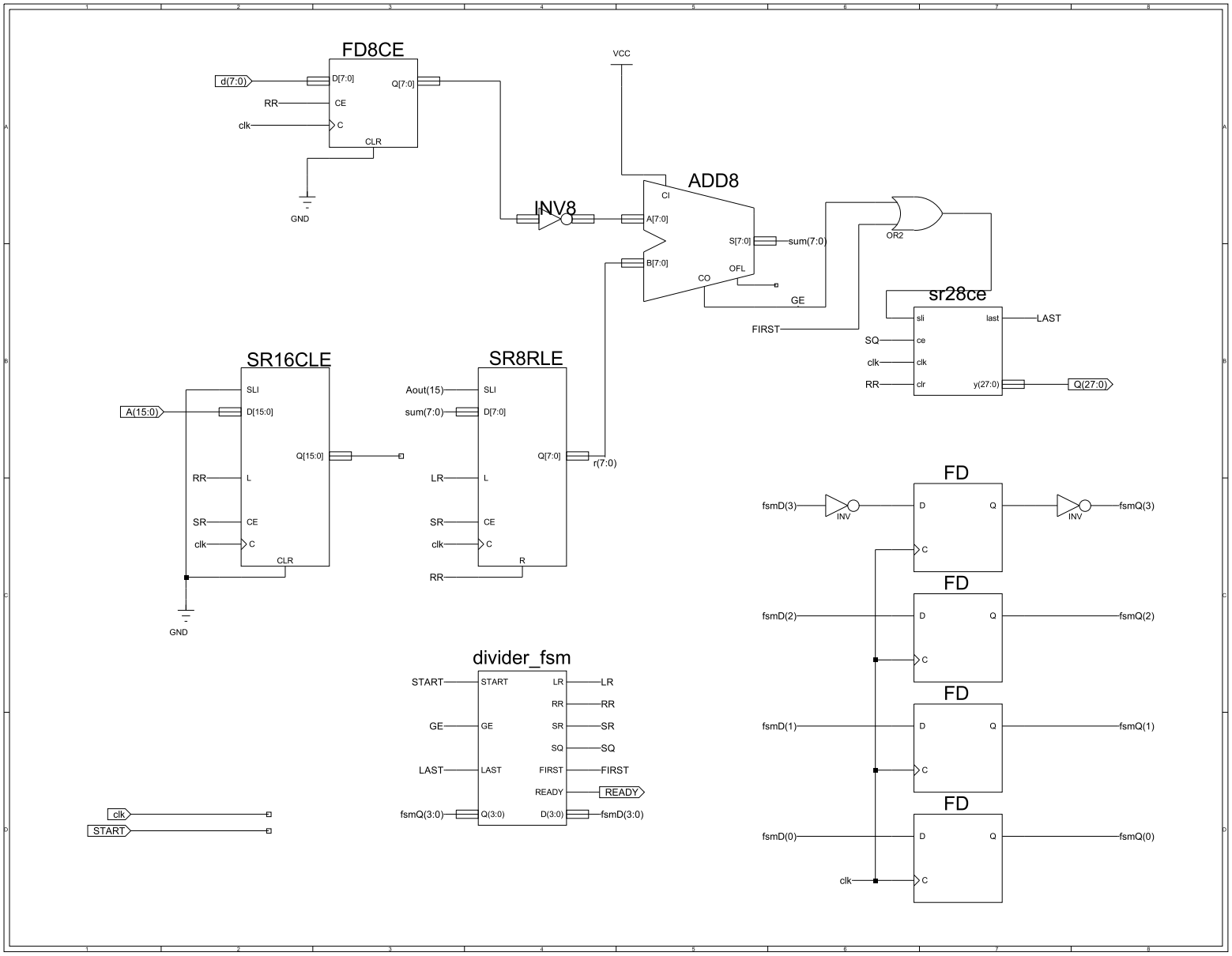
FD8CE
d(7:0)
D[7:0]
Q[7:0]
RR
CE
clk
C
CLR
GND
VCC
ADD8
CI
A[7:0]
B[7:0]
S[7:0]
sum(7:0)
OFL
CO
GE
INV8
OR2
sr28ce
sli
ce
clk
clr
last
y(27:0)
LAST
SQ
RR
Q(27:0)
FIRST
SR16CLE
SLI
D[15:0]
A(15:0)
Q[15:0]
RR
L
SR
CE
clk
C
CLR
GND
SR8RLE
Aout(15)
sum(7:0)
SLI
D[7:0]
Q[7:0]
r(7:0)
LR
L
SR
CE
clk
C
R
RR
FD
fsmD(3)
INV
D
Q
C
fsmQ(3)
fsmD(2)
fsmQ(2)
fsmD(1)
fsmQ(1)
fsmD(0)
fsmQ(0)
clk
divider_fsm
START
GE
LAST
fsmQ(3:0)
Q(3:0)
LR
RR
SR
SQ
FIRST
READY
D(3:0)
fsmD(3:0)
clk
START